

FIG. 1 RELATED ART

• SWITCHING REGULATOR

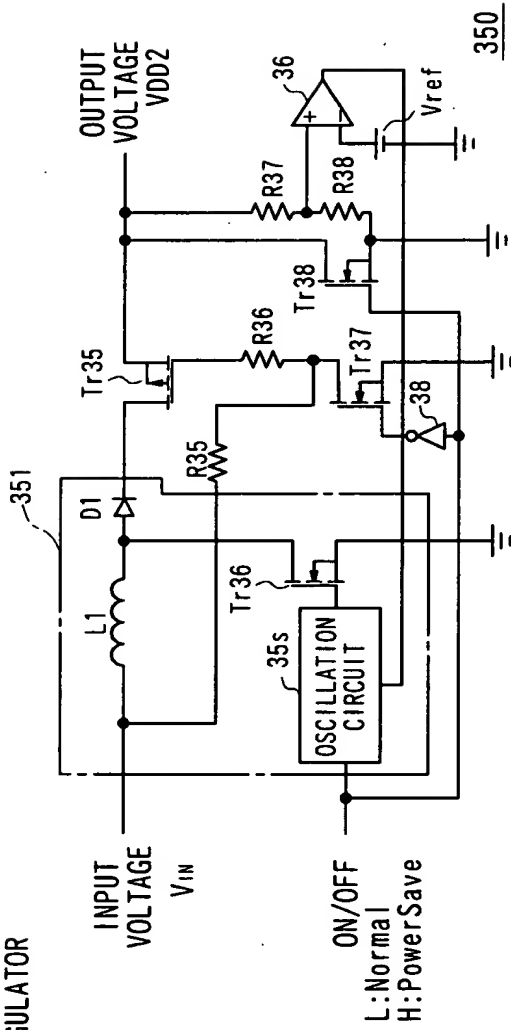


FIG. 2A RELATED ART

• CHARGE PUMP TYPE

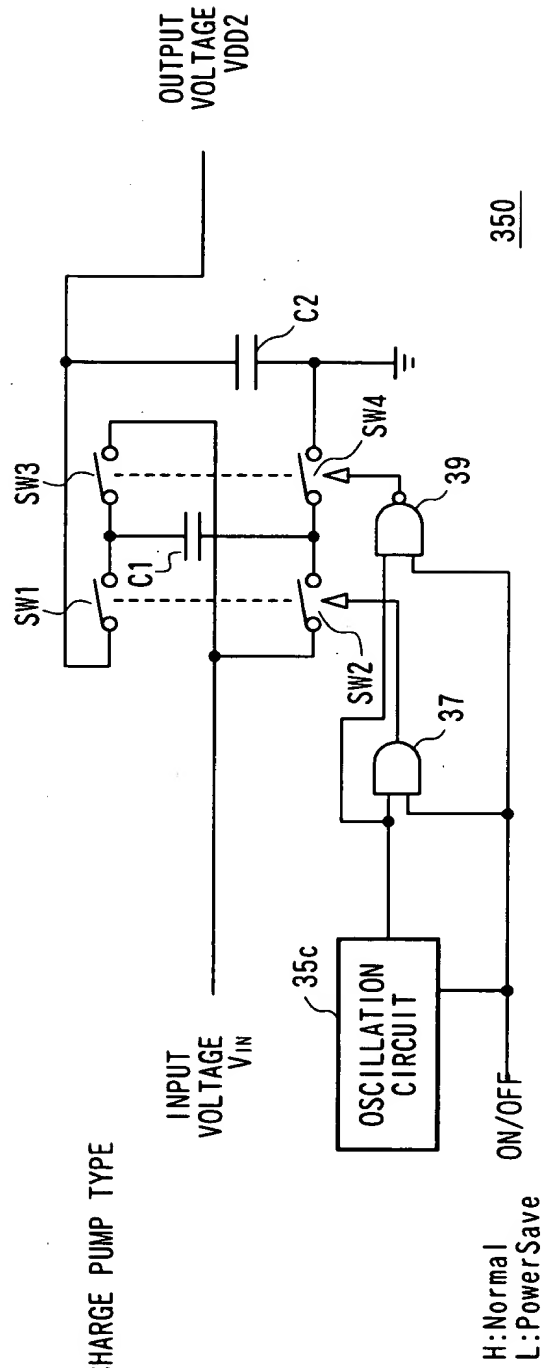


FIG. 2B RELATED ART

FIG. 3 is a block diagram of a system 100 according to an embodiment of the present invention.

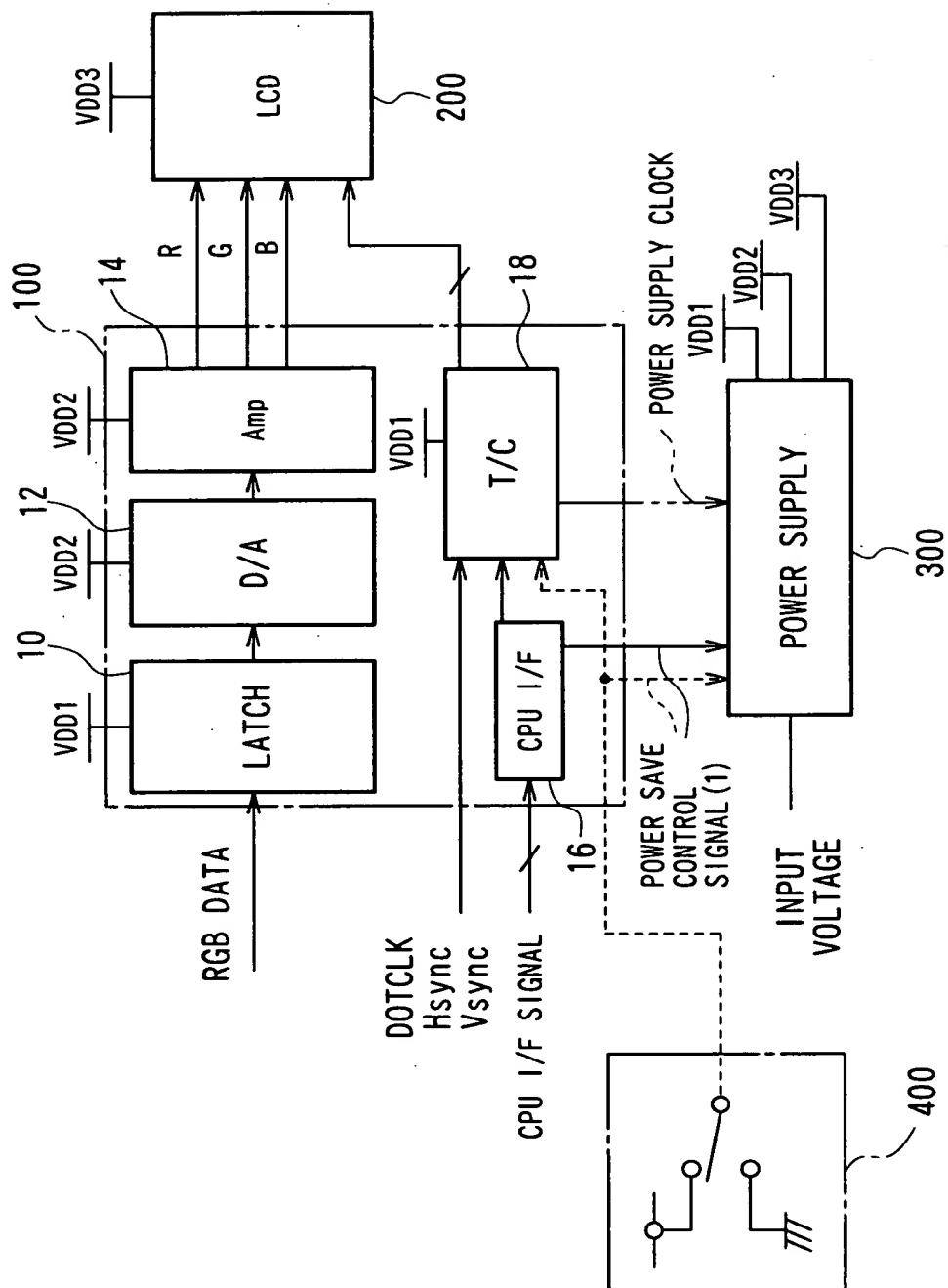


FIG. 3

Year	1950	1951	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1950	1950	1951	1952	1953	1954	1955	1956	1957	1958	1959	1960	1961	1962	1963	1964	1965	1966	1967	1968	1969	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100



• CHARGE PUMP TYPE

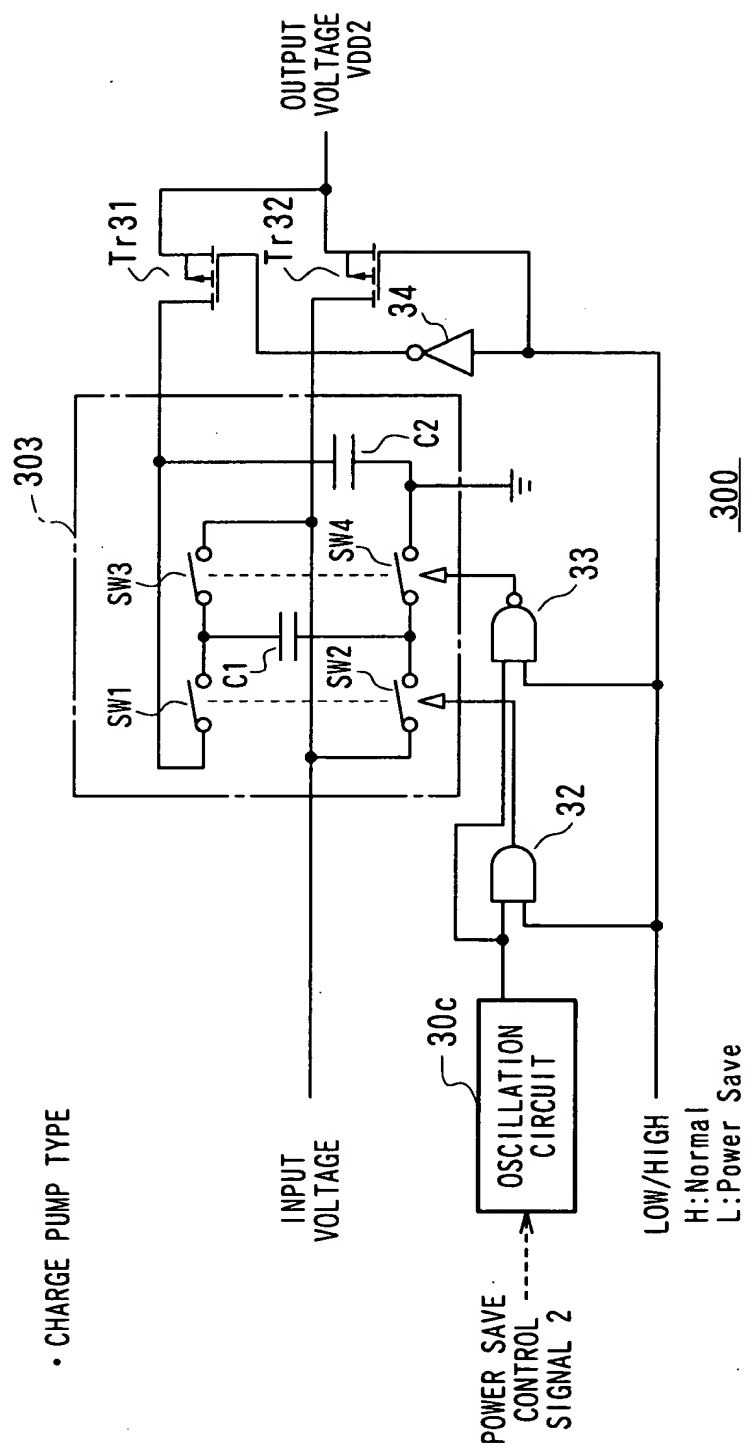


FIG. 5

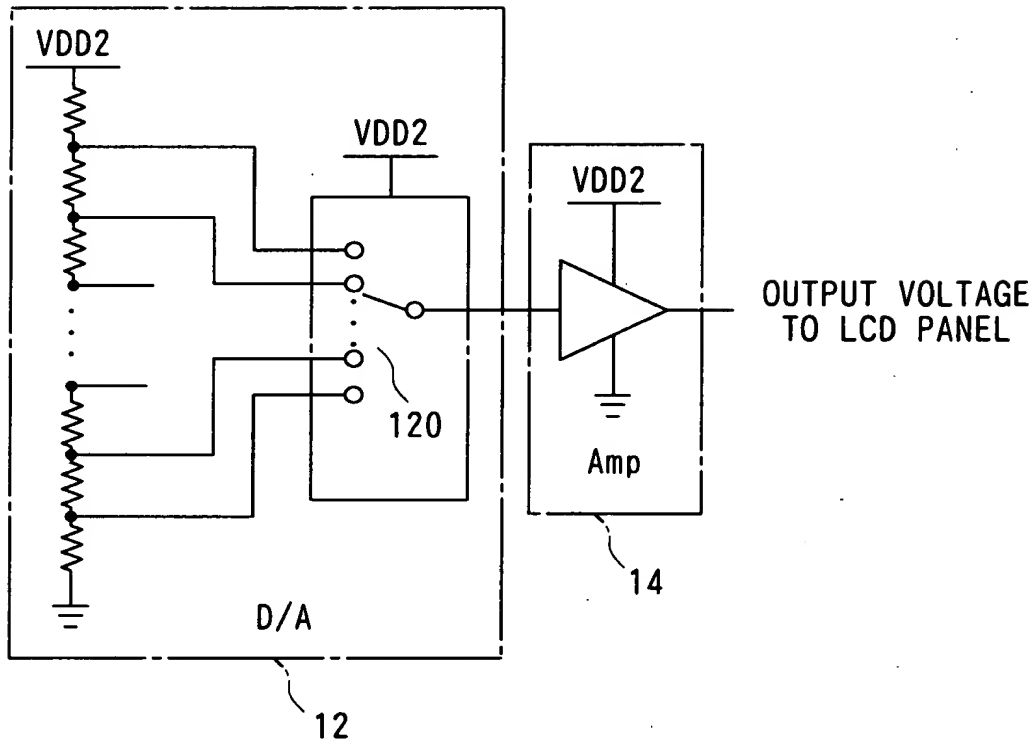


FIG. 6

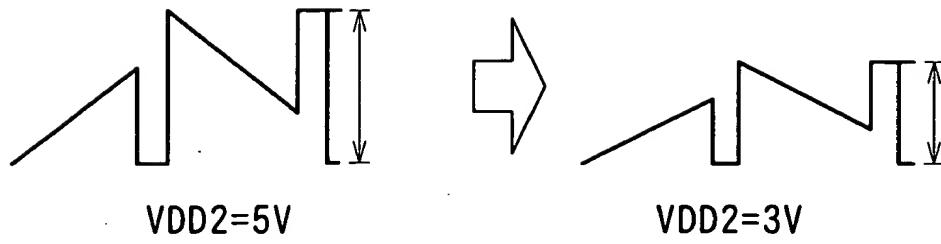


FIG. 7

FIG. 8 is a schematic diagram of a charge pump circuit 300. The circuit includes an input voltage V_{in} and an output voltage V_{DD2} . The circuit is controlled by a power supply clock (C) and a power save control signal 1 (A). The circuit includes a charge pump circuit 303, a first PMOS transistor Tr31, a second PMOS transistor Tr32, a first NMOS transistor Tr33, a second NMOS transistor Tr34, a first capacitor C1, a second capacitor C2, a first switch SW1, a second switch SW2, a third switch SW3, and a fourth switch SW4. The charge pump circuit 303 is connected to the input voltage V_{in} and the output voltage V_{DD2} . The first PMOS transistor Tr31 is connected to the output voltage V_{DD2} and the first NMOS transistor Tr33. The second PMOS transistor Tr32 is connected to the output voltage V_{DD2} and the second NMOS transistor Tr34. The first NMOS transistor Tr33 is connected to the first capacitor C1 and the first switch SW1. The second NMOS transistor Tr34 is connected to the second capacitor C2 and the second switch SW2. The first capacitor C1 is connected to the first switch SW1 and the first switch SW3. The second capacitor C2 is connected to the second switch SW2 and the second switch SW4. The first switch SW1 is connected to the input voltage V_{in} and the first switch SW3. The second switch SW2 is connected to the input voltage V_{in} and the second switch SW4. The third switch SW3 is connected to the first capacitor C1 and the first switch SW1. The fourth switch SW4 is connected to the second capacitor C2 and the second switch SW2. The first switch SW1 is controlled by the power supply clock (C) and the power save control signal 1 (A). The second switch SW2 is controlled by the power supply clock (C) and the power save control signal 1 (A). The third switch SW3 is controlled by the power supply clock (C) and the power save control signal 1 (A). The fourth switch SW4 is controlled by the power supply clock (C) and the power save control signal 1 (A).

• CHARGE PUMP TYPE

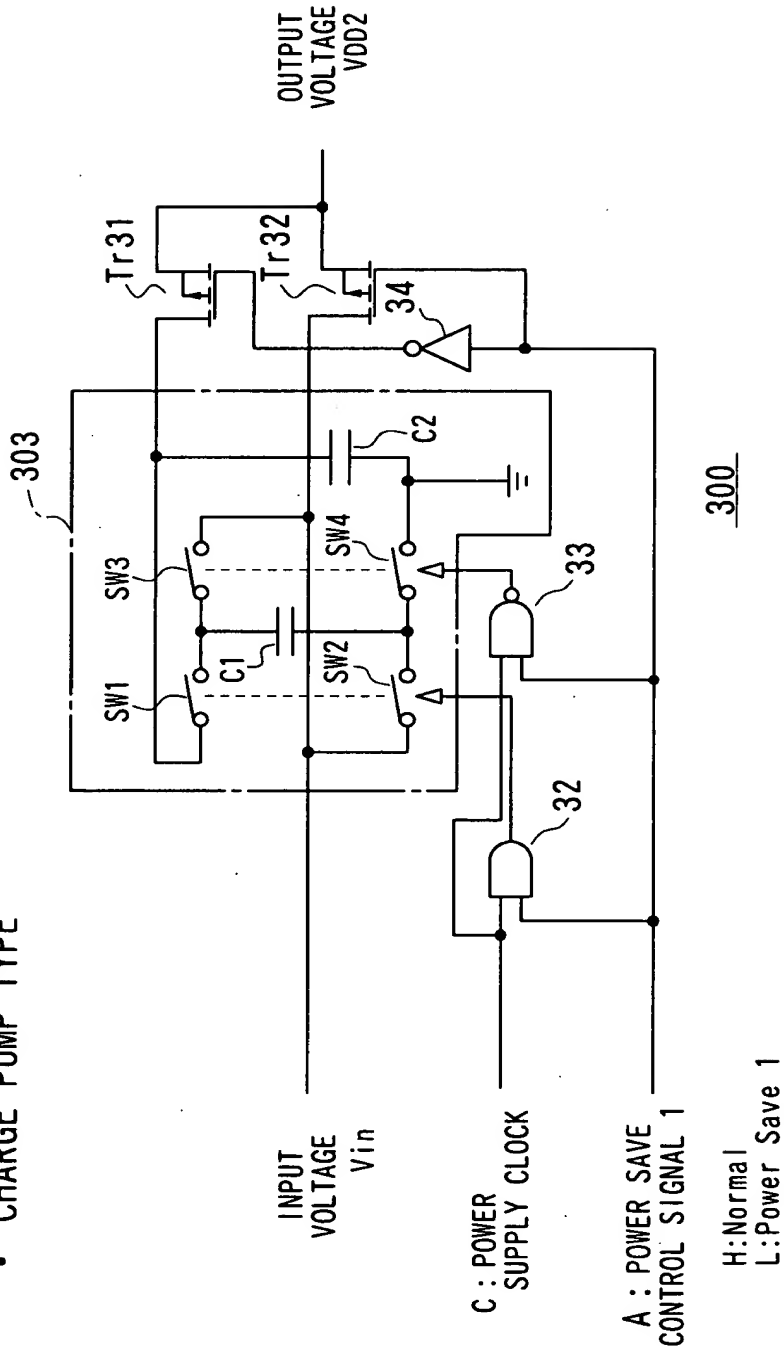


FIG. 8

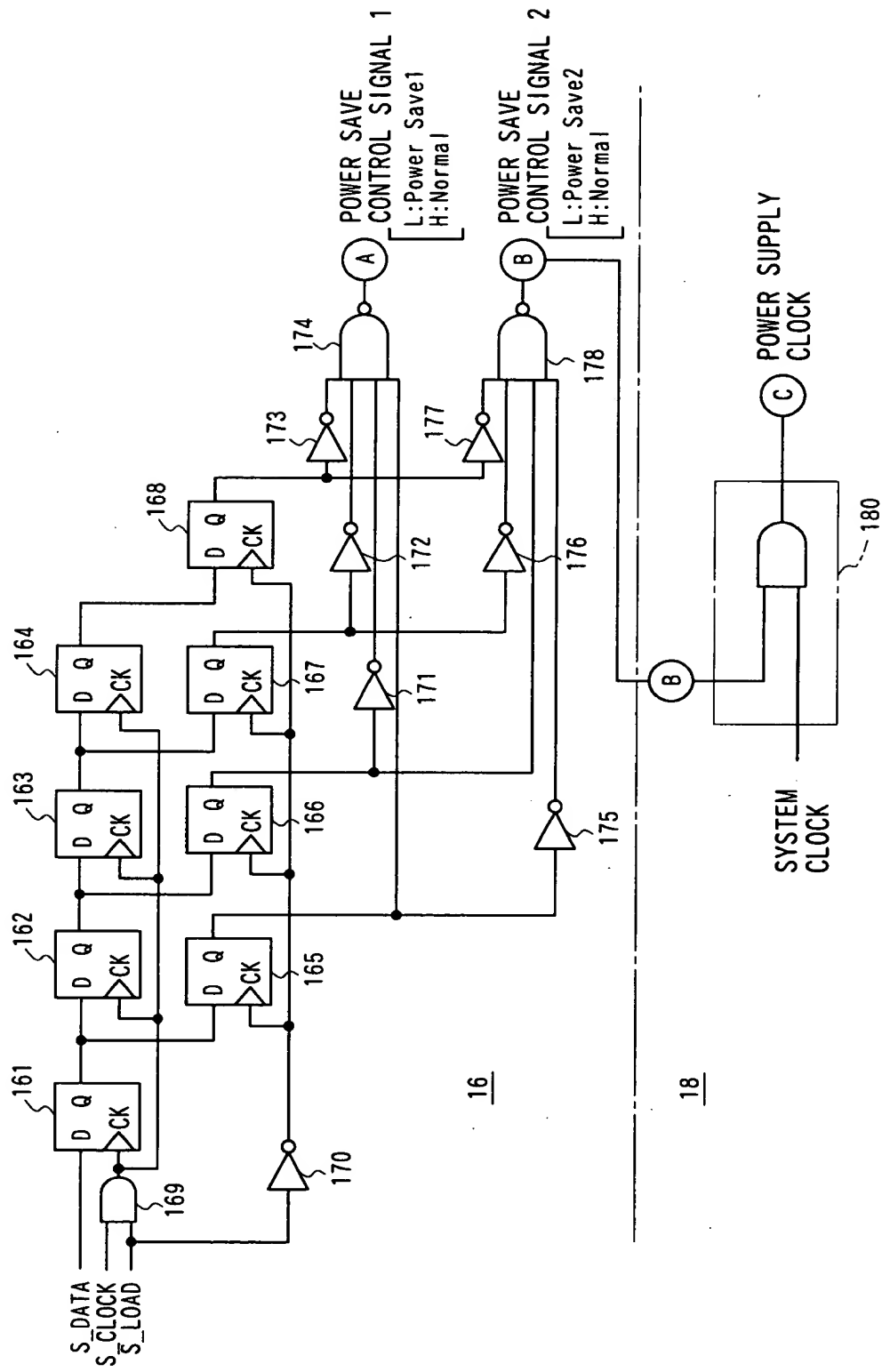


FIG. 9

POWER SAVE MODE 2 IS ACTIVATED BY
DATA 0001 (4BITS)

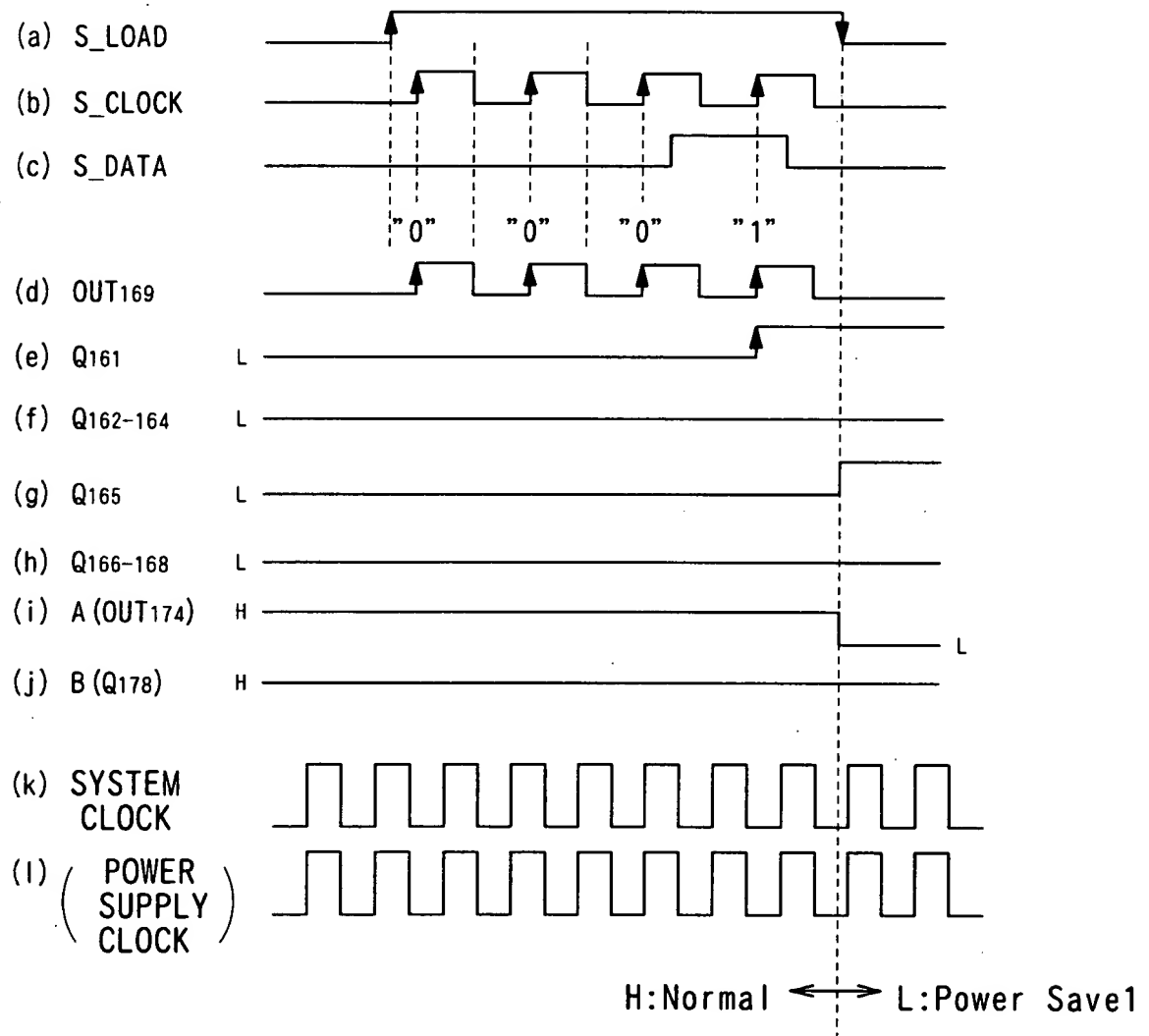


FIG. 10

POWER SAVE MODE 2 IS ACTIVATED BY
DATA 0010 (4BITS)

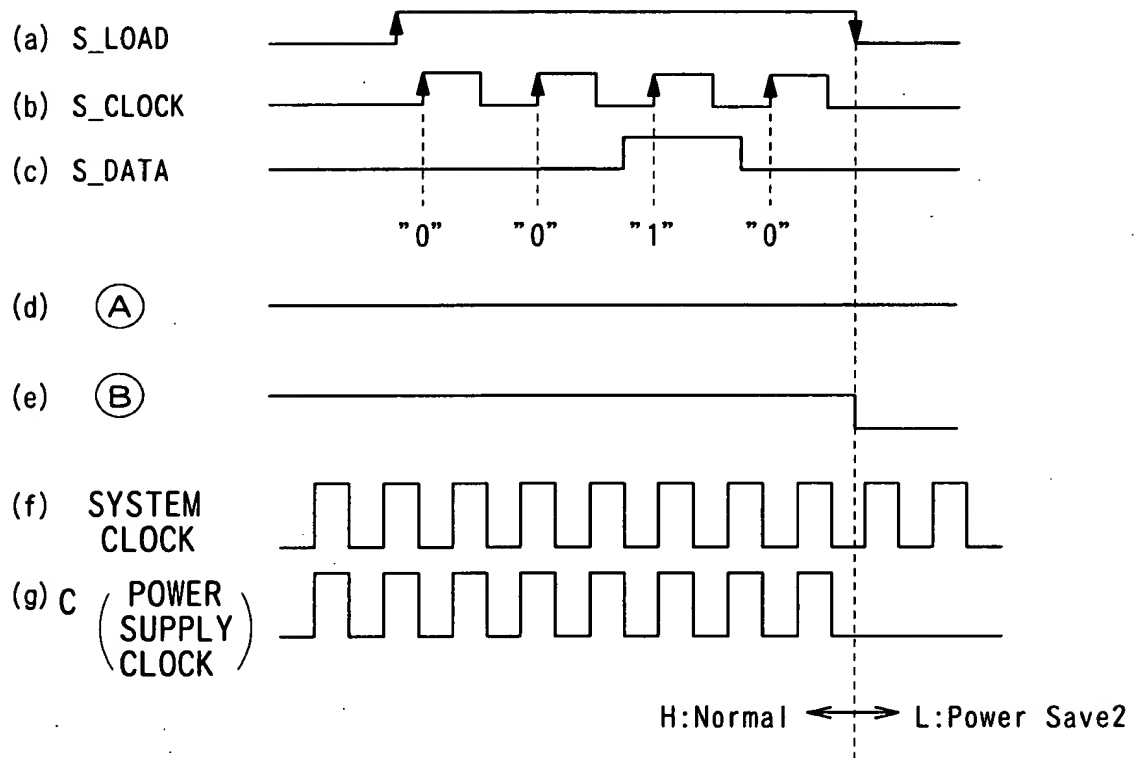


FIG. 11